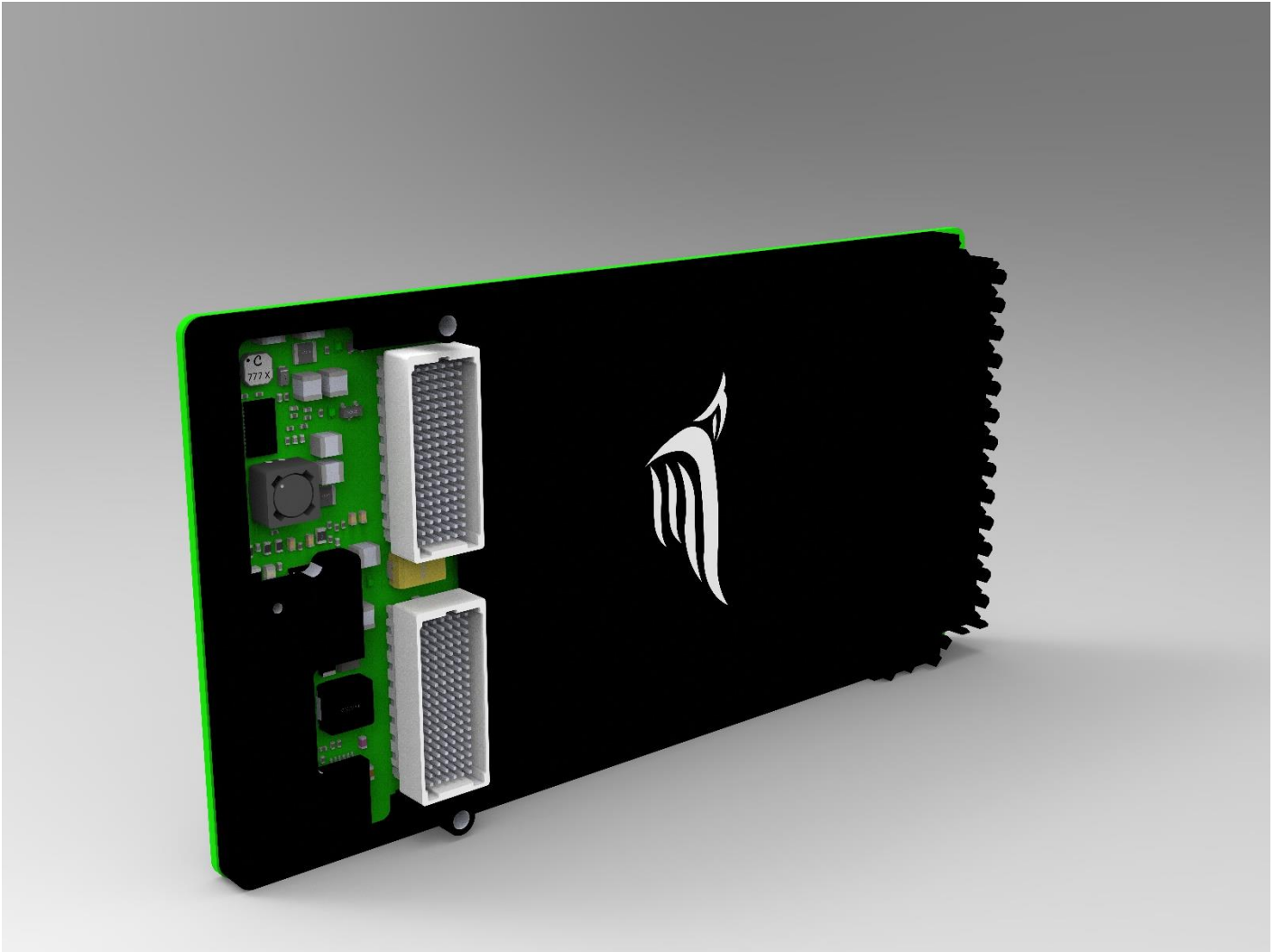




**High Speed Acoustic AWG and Signal Generator  
XMC (Switched Mezzanine Card), Rugged interface VITA 42 (XMC 1.0)**

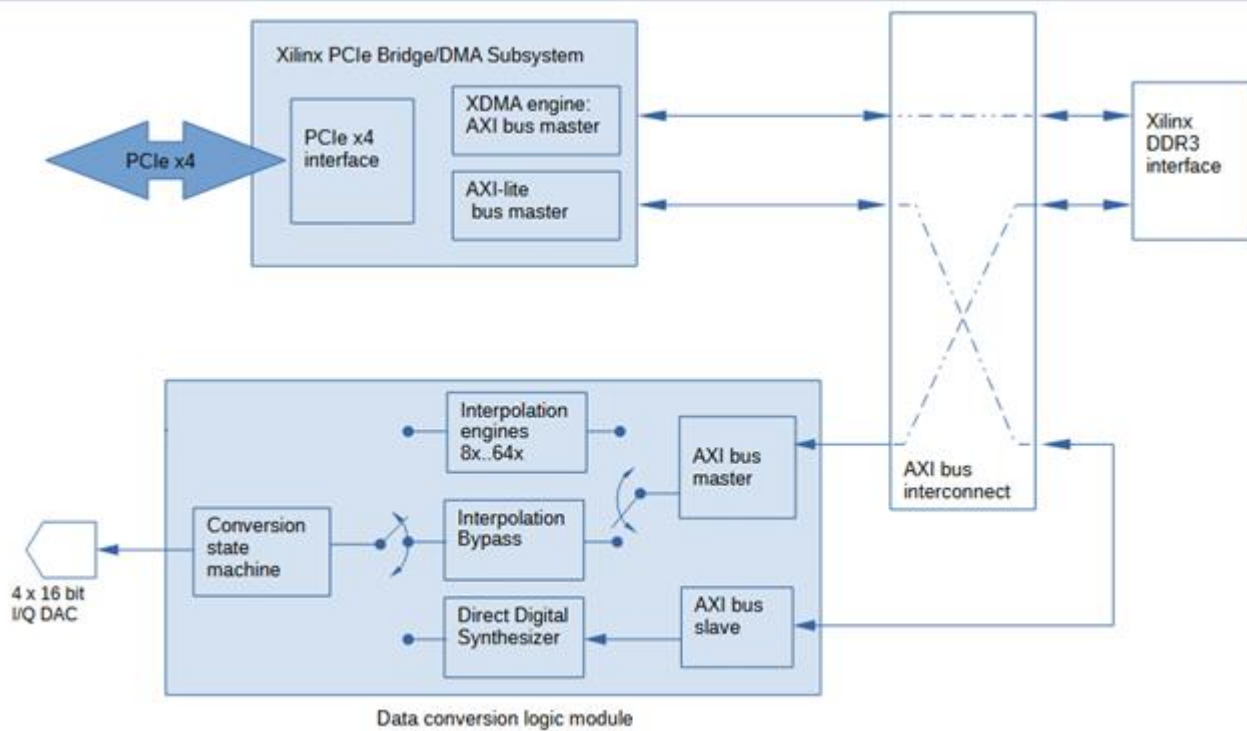


- ❖ Eight channel signal generators in XMC on RF MMCX (Micro-Miniature Coaxial).
- ❖ 16-bit I/Q DACs. Sample rate programmable up to 200 MSPS.
- ❖ On board interpolation filters and direct digital synthesizer in FPGA logic.
- ❖ 4 lane Gen 2 PCI Express interface with DMA engine, 256MB waveform memory

The **XMC16DAC8** is an eight-channel high frequency (HF) signal generator in half-length half-height PCIe form factor. The card provides eight fully differential analog output channels, which are sourced from synchronous 16-bit DACs which may be clocked at up to 200MHz. The analog output is fixed at 20Vp-p differential for full scale digital inputs, and includes two pole reconstruction filtering. All other processing is performed using the on-board FPGA resources.

The **XMC16DAC8** includes a high precision frequency synthesizer which allows the user to generate a sample clock of virtually any frequency. It can also accept an external clock for frequency coherent synchronization to peripheral equipment. When using the **XMC16DAC8**, data acquisition may be performed in either loop, pulse, or continuous mode. In pulse mode a specific number of samples are converted following a trigger event. In loop mode a specified buffer (up to 16M samples) in local memory is repetitively fed to the converters. Continuous mode allows the user to feed data from the host system over the PCIe interface. The amount data acquired is virtually unlimited, but the data rate will be limited by the bandwidth of the PCIe connection. Conversion may be initiated and terminated by software commands, or by the external trigger/gate input.

## Architecture



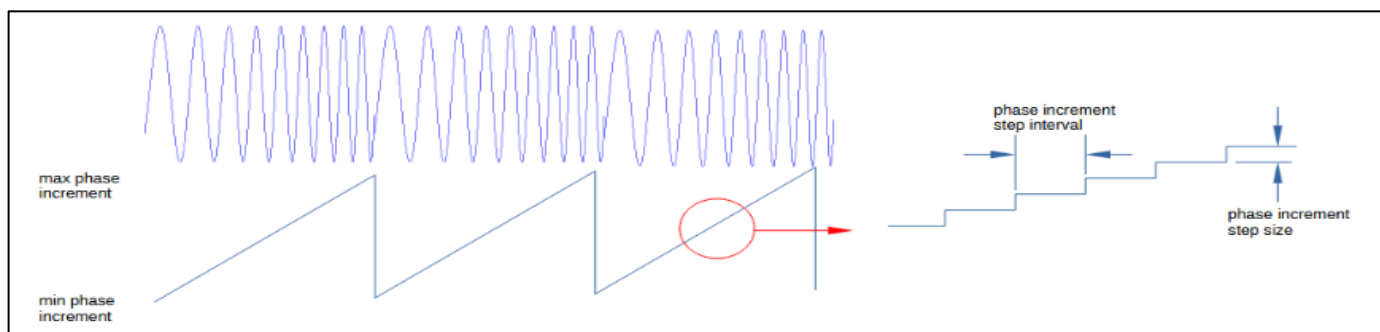
## On board processing

The **XMC16DAC8** includes on board processing resources to support operation as a multi-channel AWG or signal generator. The card can accept data streamed from a host processor in real time, it can operate on previously buffered data, or it can generate it's own waveform data based on a direct digital synthesis core.

A key component of the **XMC16DAC8** DSP capability is the interpolation engines. These allow the user to supply data at the rate determined by the bandwidth of the signal to be generated, regardless of the DAC conversion rate. The interpolated data effectively represents the signal of interest at a higher oversampling ratio. This increases the separation between the generated signal and its image(s), simplifying task of the reconstruction filter.

Arbitrary waveforms may be stored in the on board 256MB DRAM, and the played out through the DACs based on software commands or trigger signals supplied from external hardware.

Some applications may require waveforms that can be efficiently (re)created using direct digital synthesis. The **XMC16DAC8** includes a DDS that the user can configure from the API. The user can generate an FM chirp by specifying the start and stop frequencies, the frequency step size, and the dwell time.



## Target Specifications:

### Architecture and Functionality

- ❖ Sigma-delta data acquisition card in XMC Form Factor
- ❖ 256 MB DDR3 DRAM memory.
- ❖ Xilinx Artix 7 FPGA: Artix 7
- ❖ QSPI Flash memory for FPGA configuration, calibration data, etc.
- ❖ Supports continuous, pulse, and loop modes of operation.
- ❖ x4 PCI Express (Gen 2). Includes DMA engine with 64 bit addressing capability.
- ❖ Total power dissipation approximately 9W. (estimated)

### Analog Outputs

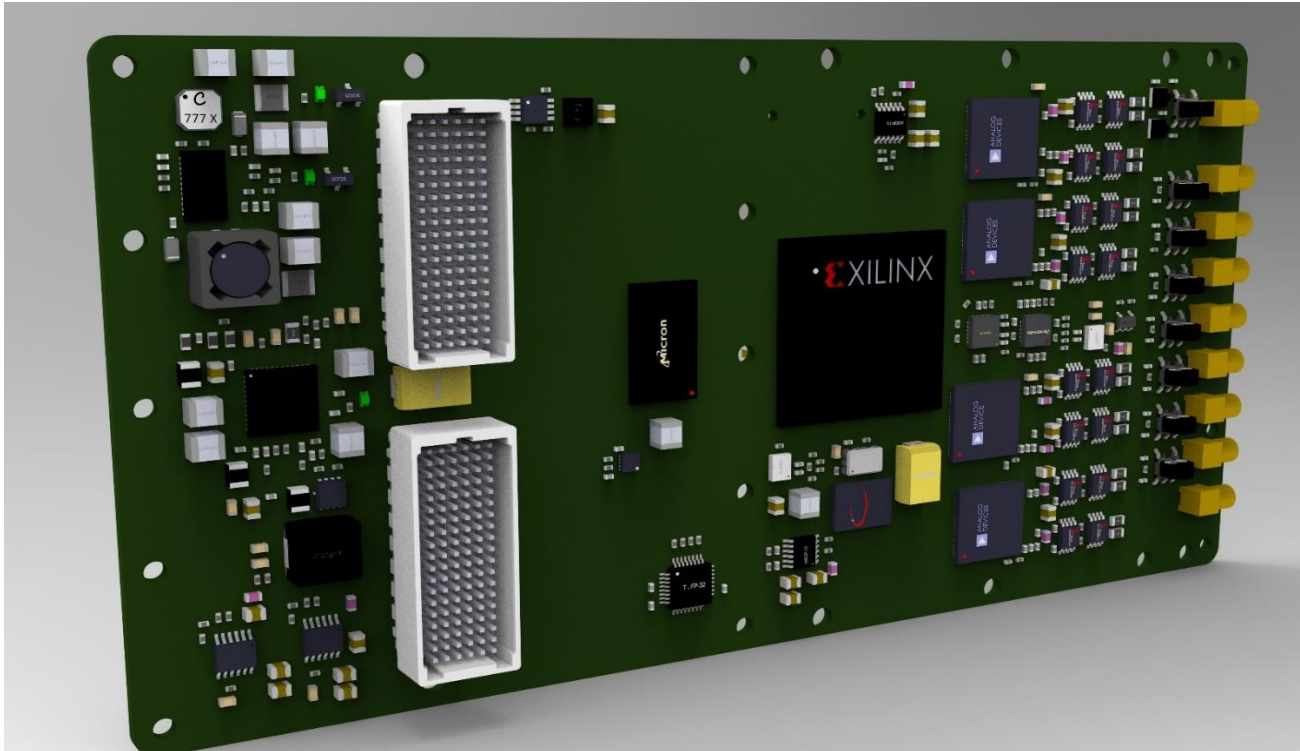
- ❖ 8 analog output channels. Can be used independently, or as 4 complex (I/Q) channels.
- ❖ 50 Ohm output impedance. Two pole low pass anti-alias filter.  $F_c$  10 MHz
- ❖ Fixed 20Vp-p differential output at full scale digital input. Contact factory if a different value is required.
- ❖ 16-bit DAC I/Q DACs. Sample rate programmable up to 200 MSPS.
- ❖ Noise spectral density  $< 150\text{dBc/Hz NSD}$  (10MHz out @ 200MSPS)
- ❖ SFDR  $> 79\text{dB}$  (10MHz output signal @ 100MSPS input data rate)
- ❖ Analog IO uses MMXC connectors. Front panel or rear IO (VITA67) options available

### On board DSP

- ❖ Interpolation blocks provide options for reduced input data rates.
- ❖ Programmable output delay simplifies transmit beam forming.
- ❖ Direct digital synthesizer (DDS) allows FMCW and chirp waveforms to be generated internally.

### Clock generation and synchronization

- ❖ On board clock synthesizer programmable with approximately 1Hz resolution.
- ❖ The clock synthesizer may be synchronized to an external reference clock (typically 10MHz).



### Integration Support

- ❖ Software Development Kit for 64-bit Linux, with application examples written in 'C'.

### Environmental

- ❖ Specifications guaranteed for operation from 0 to 50 °C.
- ❖ Storage temperature -40 to +85 °C.
- ❖ Rugged conduction-cooled variant.
- ❖ Approximately 500LFM airflow required for convection cooling