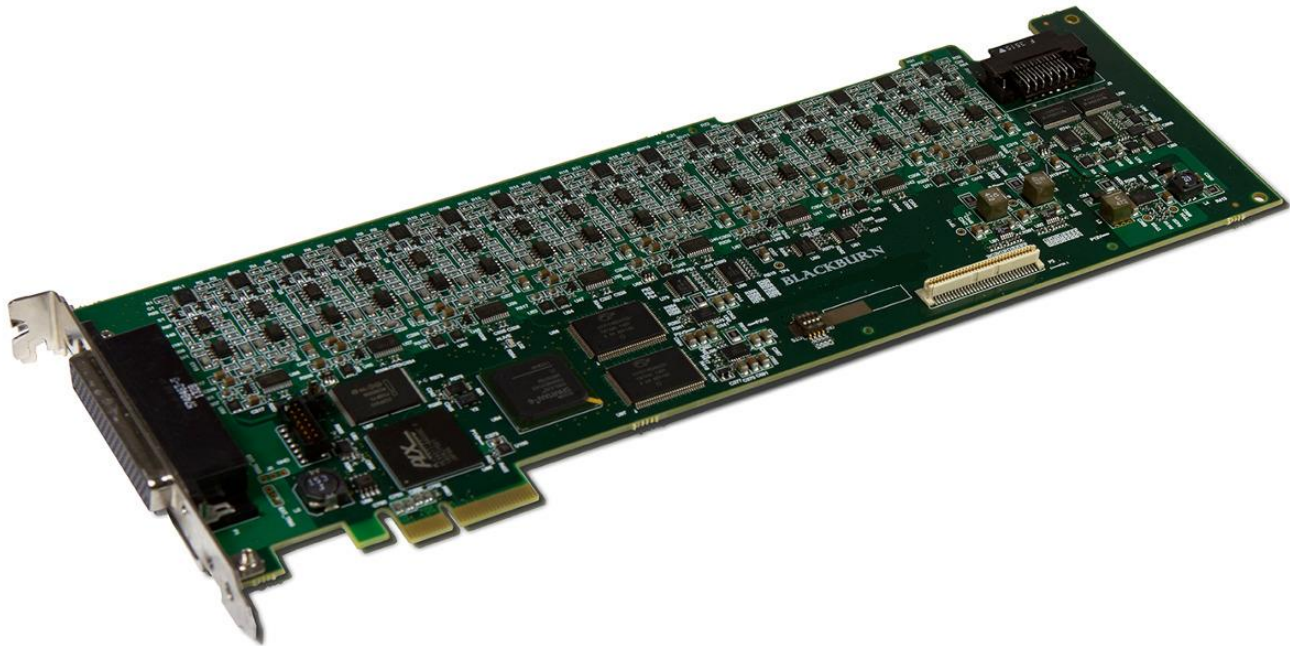




PCI32ADC24 Sensor interface 32 channel acoustic receiver for PCIe systems

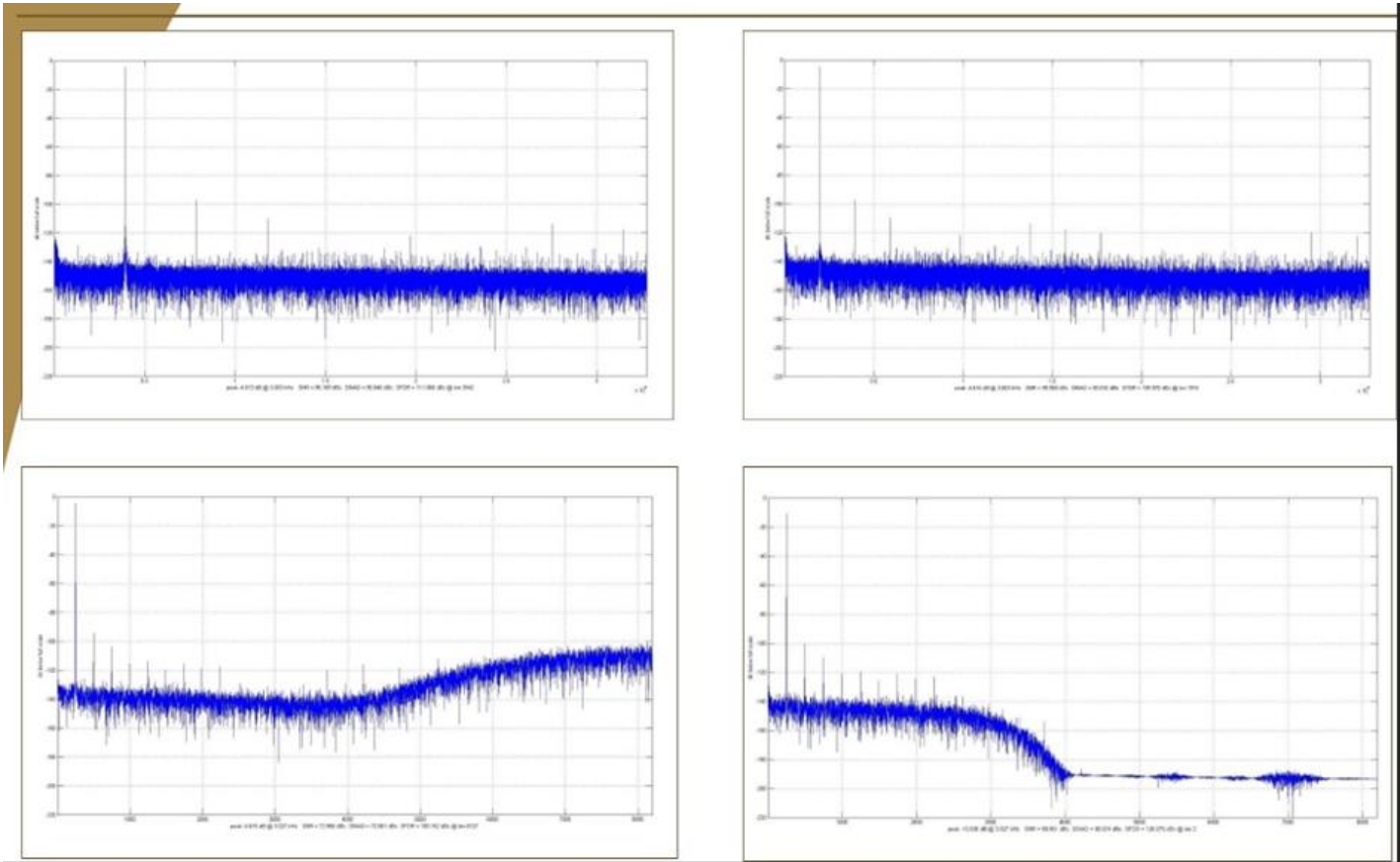


About the PCI32ADC24

The PCI32ADC24 is a sensor interface card which allows server class PCs to be deployed in a wide variety of acoustic signal processing applications, including sonar beam forming, vibration analysis, geophysics, and other test and measurement applications. This full-length PCI Express slot card accepts 32 analog input channels, which it converts to digital data with 24-bit resolution, at sample rates up to 216 kHz. The PCI32ADC24 design includes precise synchronization between multiple cards; systems can be expanded to support hundreds of channels. Minimal analog signal conditioning is used in the design: only adjustable gain and two pole anti-alias filtering. All other processing is performed using the on-board FPGA resources.

BT provides the user with a Software Development Kit (SDK) which supports application development under either the Windows or Linux operating system. The PCI32ADC24 hardware and SDK support operation in 64-bit systems, including demand mode DMA anywhere in the 64-bit addressing range. A sophisticated API provides high level hardware control functions and operating examples.

By using sigma delta ADCs, the PCI32ADC24 provides highly oversampled digital data representing of the analog input signals. Sample rates up to 54 kHz are achieved with 256x oversampling, while sample rates from 50 to 108 kHz are supported with 128x oversampling. Sample rates from 100 to 216 kHz are supported at 64x oversampling, but in order to achieve this, one filter stage in the ADC is bypassed. The front-end signal conditioning provided on the PCI32ADC24 allows the user to adjust the maximum input voltage range at run time, selecting among 1, 2, 5, and 10 V peak-to-peak (differential).



There are two signal filtering mechanisms employed in this product: a fixed two pole anti-alias filter in the analog front end and a programmable digital filter in the FPGA. The analog filtering provides anti-alias protection, and the digital filter provides a sophisticated mechanism for data rate reduction, and excision of in-band interferers. The default digital filter is a low pass configuration based on 32 coefficients, and provides a pass band flat to 30% of Nyquist, with full stop band attenuation achieved at 50% of Nyquist. Alternative configurations are available on request

The PCI32ADC24 includes a high precision frequency synthesizer which allows the user to generate a sample clock of virtually any frequency, between 8 kHz and 216 kHz, with sub-hertz precision. It can also accept an external clock for frequency coherent synchronization to peripheral equipment. When using the GB104, data acquisition may be performed in either capture or continuous mode. In capture mode a specific number of samples are acquired following a trigger event, while in continuous mode the amount data acquired is virtually unlimited. In this mode acquisition is initiated and terminated by software commands. Capture mode also includes the option to store pre-trigger data if required.

Location of individual channel samples in the data stream is ensured through the use of a swing buffer memory architecture, which re-synchronizes the data stream with the memory write address at each bank swap. Should the data stream slip, for any reason, the bank swap mechanism will ensure re-synchronization of the ADC data stream on the next frame of data.

Target Specifications:

Architecture and Functionality

- ❖ 32-channel sigma-delta ADC card in a long PCI Express form factor, full height. Can optionally be ordered in 16-channel configuration. 256MB DDR3 DRAM memory configured as a ring buffer.
- ❖ Dual SRAM banks in “swing buffer” configuration. 16 MB total storage.
- ❖ Phase coherent operation across multiple cards guaranteed.
- ❖ Supports continuous and capture modes of operation. Capture mode includes pre-trigger storage capability.
- ❖ Control and primary data interface: x1 PCI Express. Includes demand mode DMA engine with 64-bit addressing capability.
- ❖ Spartan 6 FPGA for data routing, memory control, in-band filtering, etc.
- ❖ Total power dissipation approximately 26 W.

“Analog Performance (target specification)

- ❖ 24-bit resolution ADCs.
- ❖ Differential inputs with programmable voltage range; can also accept single ended inputs.
- ❖ 4 KOhm input impedance standard, other values may be supported as build options.
- ❖ Programmable ADC sample rate: 8 kHz to 216 kHz. Sampling frequency accurate to less than 1 Hz.
- ❖ Two pole low pass anti-alias filter. Nominal Fc 90 kHz. Contact factory for other frequencies.
- ❖ >90 dB SNR
- ❖ >85 dB SINAD
- ❖ >110 dB SFDR

Integration Support

- ❖ Software Development Kit for Windows or Linux, 32 and 64 bit.
- ❖ Application examples written in ‘C’.

Environmental

- ❖ Specifications guaranteed for operation from 0 to 50 °C.
- ❖ Storage temperature -40 to +85 °C.
- ❖ Approximately 500LFM airflow required for cooling.

Optional Equipment



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